



Sheet 1 of 1

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| Form 1449* | Atty. Docket No.: 303.586US1 | Serial No. 09/320,421 |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) | Applicant: Leonard Forbes et al. | |
| | Filing Date: May 26, 1999 | Group: 2817 |

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

| **Examiner Initial | |
|-----------------------|--|
| GT | Blalock, T.N., et al., "A High-Speed Sensing Scheme for 1T Dynamic RAM's Utilizing the Clamped Bit-Line Sense Amplifier", <u>IEEE Journal of Solid-State Circuits</u> , 27(4), pp. 618-625, (April 1992) |
| GT | Kuge, S., et al., "SOI-DRAM Circuit Technologies for Low Power High Speed Multigiga Scale Memories", <u>IEEE Journal of Solid-State Circuits</u> , 31(4), pp. 586-591, (April 1996) |
| GT | Parke, S.A., "Optimization of DRAM Sense Amplifiers for the Gigabit Era", <u>IEEE, Proceedings of the 40th Midwest Symposium on Circuits and Systems</u> , Sacramento, CA, pp. 209-212, (1997) |
| GT | Suma, K., et al., "An SOI-DRAM with Wide Operating Voltage Range by CMOS/SIMOX Technology", <u>IEEE Journal of Solid-State Circuits</u> , 29(11), pp. 1323-1329, (November 1994) |

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*Substitute Disclosure Statement Form (PTO-1449)

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